

# Supernodal Analysis Revisited

## (2009 Re-Release)

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**Abstract**—In this paper we show how to extend the known algorithm of nodal analysis in such a way that, in the case of circuits without nullors and controlled sources (but allowing for both, independent current and voltage sources), the system of nodal equations describing the circuit is partitioned into one part, where the nodal variables are explicitly given as linear combinations of the voltage sources and the voltages of certain reference nodes, and another, which contains the node variables of these reference nodes only and which moreover can be read off directly from the given circuit. Neither do we need preparational graph transformations, nor do we need to introduce additional current variables (as in MNA). Thus this algorithm is more accessible to students, and consequently more suitable for classroom presentations.

**ACM Classification:** I.1 Symbolic and algebraic manipulation; J.2 Physical sciences and engineering

**Mathematics Subject Classification (2000):** Primary 94C05; Secondary 94C15, 65W30

**Keywords:** analog circuits, (super-)nodal analysis, contracted graph, paths, algorithm.

### I. INTRODUCTION

It is a well known fact – already taught in most undergraduate courses on circuit theory [1] – that, when the node equations for a standard *Nodal Analysis* (NA) of a linear circuit containing only admittances and independent current sources are set up in matrix form

$$\mathbf{Y}_n \mathbf{v}_n = \mathbf{J}_n,$$

where  $\mathbf{v}_n$  denotes the vector of node voltages  $v_{\textcircled{1}}, \dots, v_{\textcircled{n}}$  of those nodes different from some fixed *reference node*  $\textcircled{0}$ , the entries of the *node-admittance matrix*  $\mathbf{Y}_n$  and the *node current-source vector*  $\mathbf{J}_n$  can be directly read off from the circuit itself. I.e., each diagonal term of  $\mathbf{Y}_n$  in position  $(i, i)$  is given by the sum of admittances incident with the node  $\textcircled{i}$ , each off-diagonal term in position  $(i, j)$ ,  $i \neq j$ , is described by the negative of the sum of admittances connecting the nodes  $\textcircled{i}$  and  $\textcircled{j}$ ; the  $i$ -th entry of the vector  $\mathbf{J}_n$  is the sum of all independent currents leaving or entering the node  $\textcircled{i}$  with a plus sign attached only to those currents directed toward the node and a minus sign to all the others.

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As is equally well known, while it is easy to extend nodal analysis to deal with circuits, which furthermore contain voltage controlled current sources or nullors, massive problems arise, when voltage sources of any kind have to be taken into consideration, as well. Although this obstacle has been basically overcome by the invention of the *Modified Nodal Analysis* (MNA), which gives a universal method for any kind of linear circuit, with good reasons most teachers of Electrical Engineering seem to be very reluctant to confront their students with the MNA-algorithm, especially in undergraduate courses.

Accordingly, several authors ([2, 3]) have proposed another alternative, the so-called *Supernodal Analysis* (SNA), which seems to be more accessible to students and thus has been incorporated into existing undergraduate and graduate courses<sup>1</sup> ([4, 5, 7]): Starting with a linear circuit with admittances and all kinds of independent sources, the initial set of equations can be reduced to a smaller set; these resulting SNA-equations again can be described in matrix form as

$$\hat{\mathbf{Y}}_N \hat{\mathbf{v}}_N = \hat{\mathbf{J}}_N,$$

where  $\hat{\mathbf{v}}_N$  is a vector of selected node voltages,  $\hat{\mathbf{Y}}_N$  is a matrix of admittances and  $\hat{\mathbf{J}}_N$  consists of suitably chosen linear combinations of the independent sources. Although in the literature ([3, 4]) instructions are given how to calculate the entries of  $\hat{\mathbf{Y}}_N$  and  $\hat{\mathbf{J}}_N$ , as far as we know, no algorithm has been developed, yet, which in analogy to standard nodal analysis allows one to directly read them off from the circuit. This paper was written to remedy this situation.

**Remark:** Throughout this paper, to keep notation as simple as possible, while we freely talk about circuits with admittances, all the examples will be linear circuits considered in the time domain, which besides independent sources consist of resistors with positive conductances (symbolized by capital letters), controlled sources and/or nullors. The experienced reader will know how to generalize the results, which will be presented, to other linear circuits containing inductors and capacitors.

The only notational convention we will strictly adhere to is using boldface letters for vectors and matrices.

Without loss of generality (cp. [8], 1.5.3) we demand that all circuits under consideration are connected.

### II. SUPERNODAL ANALYSIS OF LINEAR CIRCUITS WITH INDEPENDENT SOURCES

To keep matters simple at the beginning, in this section we will only consider circuits without controlled sources and

<sup>1</sup>Since the first publication of this article, the lecture notes [5] seem not to be publicly available anymore. Nevertheless, those contents of the course which were relevant for this paper have been incorporated into [6].

nullors.

The basis of our discussion is the concept of a *supernode*. The definition, we will give, slightly differs both from the one presented in [2], as well as from the one in [4], chapter 4.2. This was done to streamline the formulation of the “traditional” algorithm and to prepare for our improvements.

**Definition 1:** A subcircuit of a given circuit which is connected, consists only of nodes and (independent) voltage sources, and which is maximal with these two properties<sup>2</sup> is called a *supernode*.

Let us remark, that by this definition an ordinary node which is not incident with any voltage source is regarded as a supernode, as well. Furthermore, any supernode defines a cut of the circuit. The *contraction*<sup>3</sup>  $\hat{\Gamma}$  of a circuit  $\Gamma$ , obtained by contracting all the branches of all supernodes and removal of all resulting loops, is a circuit, which by the initial prerequisite of this section only contains resistors and independent current sources. During the course of this paper we will call  $\hat{\Gamma}$  the *contraction along the supernodes*.

If, moreover, one removes all branches associated to current sources from  $\hat{\Gamma}$ , the result is the *deactivated circuit* in the sense of [3, 4].

#### A. The Algorithm – Proceeding as in Textbooks

We are now able to adapt the general algorithm of *Supernodal Analysis* as presented in [2, 3, 4], and formulate it in our terminology.

**Input:** a connected circuit  $\Gamma$  with  $n + 1$  nodes, named  $\textcircled{0}, \textcircled{1}, \dots, \textcircled{n}$ , consisting only of independent sources and resistors. (\* Node  $\textcircled{0}$  will be our *global reference node* (ground/datum), and we set  $v_{\textcircled{0}} = 0$ . \*)

**Output:**

- 1) a set of equations for the node voltages  $v_{\textcircled{0}}, v_{\textcircled{1}}, \dots, v_{\textcircled{n}}$ , which completely describes the circuit  $\Gamma$ .
  - 2) a subset of node voltages together with a *reduced system* of equations (i.e. equations containing these variables only), the solution of which directly leads to the solution of the whole system.
- 1) Initialization
    - a) Assign node voltages.
    - b) Identify all supernodes and mark them; let  $N + 1$  be the number of nodes in the contraction along the supernodes  $\hat{\Gamma}$ .
    - c) Within each supernode define one node as the *local reference node* of the supernode (a supernode consisting of a single node only is its own reference node). The global reference node should be chosen to be a local reference node<sup>4</sup>.
  - 2) For each supernode, express the node voltages within in terms of the node voltage of its local reference node and the values of the voltage sources, it encompasses.

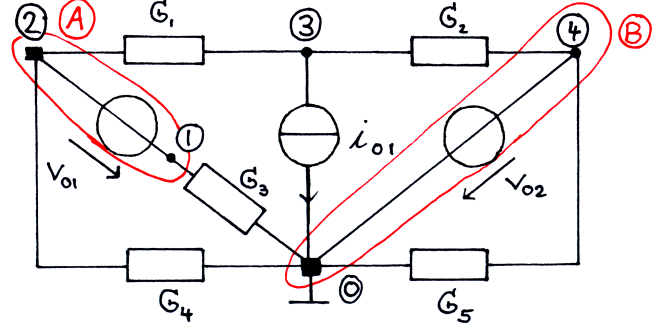
<sup>2</sup>I.e. it cannot be enlarged without losing one or the other attribute.

<sup>3</sup>in the sense of [9], exercise II.4.15.

<sup>4</sup>Clearly the global reference node need not be chosen before this step of the algorithm.

- 3) For each supernode, write one KCL equation in terms of the voltages of the local reference nodes; leave out, as usual, the one for the supernode containing the global reference node.

For those, who are not accustomed, yet, with supernodal analysis, we exemplify the workings of the above algorithm:



The two voltage sources of this circuit give rise to two supernodes  $\textcircled{A}$  and  $\textcircled{B}$  consisting of the nodes  $\textcircled{1}, \textcircled{2}$  and  $\textcircled{0}, \textcircled{4}$ , respectively. While we can freely choose  $\textcircled{2}$  as the local reference node for the supernode  $\textcircled{A}$ , the local reference node of  $\textcircled{B}$  is supposed to be the node  $\textcircled{0}$ .

With node voltages being introduced, the internal structure of the supernodes implies

$$\begin{pmatrix} v_{\textcircled{0}} \\ v_{\textcircled{1}} \\ v_{\textcircled{4}} \end{pmatrix} = \begin{pmatrix} 0 \\ v_{\textcircled{2}} - v_{01} \\ v_{\textcircled{0}} + v_{02} \end{pmatrix} = \begin{pmatrix} 0 \\ v_{\textcircled{2}} - v_{01} \\ v_{02} \end{pmatrix}, \quad (1)$$

where we have partially solved this system of equations for the voltages of those nodes, which are not reference nodes.

Kirchhoff equations for supernodes  $\textcircled{A}$  and  $\textcircled{B}$  give:

$$\begin{aligned} G_1(v_{\textcircled{2}} - v_{\textcircled{3}}) + G_3(v_{\textcircled{1}} - v_{\textcircled{0}}) + G_4(v_{\textcircled{2}} - v_{\textcircled{0}}) &= 0, \\ G_1(v_{\textcircled{3}} - v_{\textcircled{2}}) + G_2(v_{\textcircled{3}} - v_{\textcircled{4}}) + i_{01} &= 0. \end{aligned}$$

Finally, by using (1) and collecting all currents and voltages resulting from independent sources on the right hand side, we are led to the following system of equations for the voltages of the local reference nodes:

$$\begin{pmatrix} G_1 + G_3 + G_4 & -G_1 \\ -G_1 & G_1 + G_2 \end{pmatrix} \cdot \begin{pmatrix} v_{\textcircled{2}} \\ v_{\textcircled{3}} \end{pmatrix} = \begin{pmatrix} 0 & + & G_3 \cdot v_{01} \\ -i_{01} & + & G_2 \cdot v_{02} \end{pmatrix} \quad (2)$$

This reduced system is completely decoupled from (1). Furthermore its solution together with (1) describes all the node voltages of our example circuit.

#### B. On the results of the SNA algorithm in general

The preceding example gives rise to some observations, which easily generalize to theorems for arbitrary circuits built from admittances and independent sources. Let us suppose that within each supernode one local reference node has already been chosen.

**Theorem 2:** If a supernode carries the structure of a tree then the voltage of any node within the supernode is uniquely

expressible as the voltage of the local reference plus the sum, relative to the path orientation, of voltages of those independent sources along the unique path from the reference node to the node under consideration.

Thus, step 2 of the algorithm can be successfully carried out, iff either every supernode is a tree, or any loop of independent voltage sources within any supernode satisfies KVL (which can be easily checked by identifying a spanning tree within each supernode).

For the sake of completeness, we note that branch voltages along admittances which at both ends are incident with the same supernode can be determined without any calculations.

**Theorem 3:** If one of the above assumptions holds, the system of equations resulting from step 3 of the algorithm of supernodal analysis can be reduced to

$$\hat{\mathbf{Y}}_N \hat{\mathbf{v}}_N = \hat{\mathbf{J}}_N, \quad (3)$$

where  $\hat{\mathbf{v}}_N$  is the vector of voltages of local reference nodes,  $\hat{\mathbf{Y}}_N$  is the node-admittance matrix of the contraction along the supernodes  $\hat{\Gamma}$  and  $\hat{\mathbf{J}}_N$  is a vector of currents induced by the independent sources, which will be specified more precisely below.

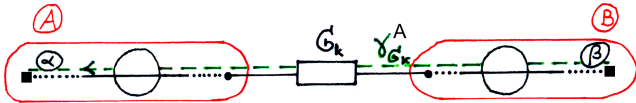
### C. Reading off the Entries from the Circuit

Since  $\hat{\mathbf{Y}}_N$  is the node-admittance matrix of the contraction  $\hat{\Gamma}$ , there is a simple rule how to fill in the entries just by inspection.

**Rule 1:** Each element on the main diagonal at position  $(A, A)$  is the sum of the admittances incident at only one end<sup>5</sup> with the supernode  $(A)$ . The off-diagonal elements at position  $(A, B)$  is the negative of the sum of those admittances connecting supernodes  $(A)$  and  $(B)$ .

In the future – for obvious reasons – when we talk about admittances “incident with a supernode” we will only consider those, that are incident at only one end.

Without loss of generality, let us assume that all supernodes of  $\Gamma$  are trees. By this additional assumption paths within each supernode are unique. Thus any admittance  $G_k$  connecting two supernodes  $(A)$  and  $(B)$  defines a unique oriented path  $\gamma_{G_k}^A$ , consisting only of independent voltage sources and the admittance  $G_k$  itself, as sketched in the figure below:



The path  $\gamma_{G_k}^A$  is uniquely defined as the path which starts in the local reference node  $(\beta)$  of  $(B)$ , passes through the node of  $(B)$  incident with the admittance  $G_k$ , along  $G_k$  to that node of  $(A)$  incident with the other end of  $G_k$  and finally ends in the local reference node  $(\alpha)$  of  $(A)$ . When this path is traversed in the opposite direction, we will call it  $\gamma_{G_k}^B$ . Now let  $\Sigma_k^A$  be the sum, relative to the orientation of this path, of those voltage

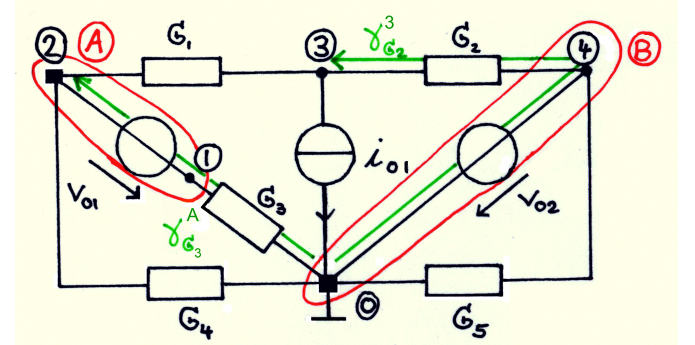
sources which are part of the path  $\gamma_{G_k}^A$ , with a voltage being counted positive if the voltage source in question and the path are oriented in opposite and negative, when the orientations are the same. Consequently we have  $\Sigma_k^A = 0$ , if  $G_k$  directly connects two local reference nodes. We are now in a position to formulate the fill-in rule for the vector  $\hat{\mathbf{J}}_N$ :

**Rule 2.** Let  $\{i_m\}$  be the current sources and  $\{G_k\}$  be the admittances of the circuit  $\Gamma$ . Let  $(A)$  be a supernode in  $\Gamma$ , not containing the datum node. Then the entry of  $\hat{\mathbf{J}}_N$  at position  $A$  is given by

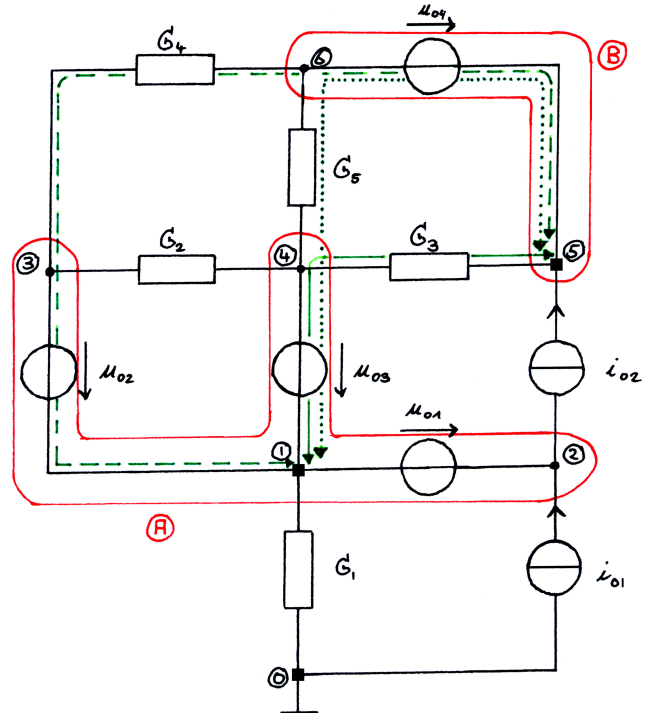
$$\sum_{i_m: i_m \rightarrow (A)} i_m - \sum_{i_r: i_r \leftarrow (A)} i_r + \sum_{G_k: G_k \text{ incident with } (A)} G_k \cdot \Sigma_k^A, \quad (4)$$

where  $i_m \rightarrow (A)$  means, that the current source  $i_m$  is incident with  $(A)$  and directed toward  $(A)$ , and  $i_r \leftarrow (A)$  that  $i_r$  is incident with  $(A)$  but directed away from  $(A)$ .

Returning to our first example, in the next figure we see the relevant paths  $\gamma_{G_2}$  and  $\gamma_{G_3}$ , which result in the entries  $G_2 \cdot v_{02}$  and  $G_3 \cdot v_{01}$  of the right hand side of equation (2).



For the convenience of our readers we give a second example with the supernodes marked and the relevant “admittance paths” sketched.



<sup>5</sup> As noted above, those admittances incident with only one supernode at both ends have to be neglected.

Now it is easy to read off the resulting reduced system of equations. The interested reader is called upon to check each entry by using the original algorithm, to see the advantage of our approach.

$$\begin{pmatrix} A \\ B \end{pmatrix} \begin{pmatrix} G_1 + G_3 + G_4 + G_5 & -G_3 - G_4 - G_5 \\ -G_3 - G_4 - G_5 & G_3 + G_4 + G_5 \end{pmatrix} \cdot \begin{pmatrix} v_{\textcircled{1}} \\ v_{\textcircled{5}} \end{pmatrix} = \begin{pmatrix} i_{01} - i_{02} & + & G_5(u_{04} - u_{03}) + G_4(u_{04} - u_{02}) - G_3 u_{03} \\ i_{02} & + & G_5(u_{03} - u_{04}) + G_4(u_{02} - u_{04}) + G_3 u_{03} \end{pmatrix}$$

Although this exemplary circuit is highly artificial, it helps to stress yet another point, namely that in many circuits any try to set up nodal equations with the help of source shifting and substitution by Norton equivalent subcircuits is highly difficult or nigh impossible.

#### D. Circuits with Controlled Sources

The algorithm of nodal analysis can be easily generalized to circuits containing voltage controlled current sources. Clearly supernodal analysis and the two rules given above are suitable for setting up the equations when circuits with voltage controlled sources of any kind have to be analyzed. In this case, however, the concept of a supernode has to be extended in the following way:

*Definition 4:* A subcircuit of a circuit which is connected, consists only of nodes and independent as well as the controlled branches<sup>6</sup> of dependent voltage sources, and which is maximal with these two properties is called a *supernode*.

By temporarily treating controlled voltage sources as independent sources (the “taping” of [4]) and using this modified definition, again we can use the above algorithm plus our two fill-in rules. To complete the algorithm, in an additional fourth step we need to replace the dependent voltages and currents by the controlling node voltages (i.e. the untaping of [4]). In this more general case, we cannot expect a clean-cut partition of the node equations into those, describing the “inner workings” of each supernode and those resulting from the contracted circuit only. Nevertheless, our rules lead to a simple to set up interim result.

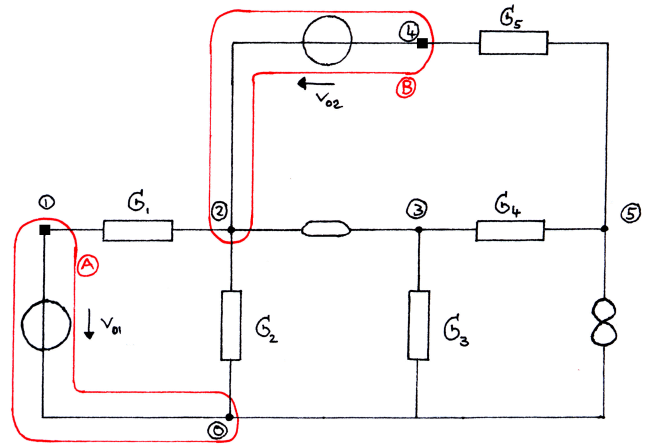
Let us finally consider current controlled sources: When supernodes have been introduced, controlling branch currents fall into two classes, those inside and those outside a supernode. Those outside are currents through admittance branches and thus can be easily substituted by the corresponding set of node voltages as variables. In the second case, with the controlling branch being part of a supernode, if again we can assume that each supernode is a tree, then by induction we can show that at least one end of the branch under consideration has to be the root of a rooted tree of voltage sources. The leaves of this tree are nodes through which currents induced by admittance branches or current sources enter the supernode. Now, using KCL at each node of the rooted tree, it is easy to describe the controlling branch current as the sum of all of these currents.

<sup>6</sup> The reader should keep in mind that a controlled source consists of two branches; thus we have to specify which branch should belong to the supernode.

### E. Circuits which contain Nullors

It was the authors initial hope that the approach of supernodal analysis by inspection could somehow be made to work on circuits containing nullors as well. This hope was shattered by the example below<sup>7</sup>.

Though for circuits containing nullors, again there is a reduced equation system which is of the form  $\hat{\mathbf{Y}}_N \hat{\mathbf{v}}_N = \hat{\mathbf{J}}_N$  and although there are hints of how to fill out  $\hat{\mathbf{Y}}_N$ , in general there does not seem to be any suitable definition of the notion of a supernode which would lead to a short cut, by which the tedious setting-up of equations could be avoided: On the one hand supernodes in circuits with nullors should contain the norators (thus defining Kirchhoff-surfaces for which the equations have to be set up); on the other hand the voltages of nodes connected by nullators to supernodes (in the sense of definition 1) are known from the beginning as well, and should not appear as variables in their own right. As our example shows, these two demands do not lead to any well to teach or easy to apply fill in rule.



$$\frac{\textcircled{B}}{\textcircled{3}} \quad \begin{pmatrix} -(G_1 + G_2) & G_1 + G_2 + G_5 & -G_5 \\ -G_3 & G_3 + G_4 & -G_4 \end{pmatrix} \cdot \begin{pmatrix} v_{\textcircled{1}} \\ v_{\textcircled{4}} \\ v_{\textcircled{5}} \end{pmatrix} = \begin{pmatrix} -G_2 \cdot v_{01} + (G_1 + G_2) \cdot v_{02} \\ -G_3 \cdot v_{01} + (G_3 + G_4) \cdot v_{02} \end{pmatrix}$$

Fortunately, in case of admittance circuits with nullors, supermesh analysis or RLA, as it was presented in algorithm 3.2 and chapter 5 of [2] can be shown to be universal, and thus can be used for all circuits without cutsets of independent current sources and nullators.

### III. CONCLUSION

Past experience in Braunschweig with an undergraduate course of about 150 students [7] has shown that the modified SNA-algorithm, with fill-in rules, as presented above, is quite easy to teach. Moreover, the students naturally adapted

<sup>7</sup>The reader should note the particular choice of nodes ① and ④ as local reference nodes, which from a practical point of view clearly is absurd, but from an algorithmic point of view is a distinct possibility. Furthermore we have refrained from setting  $v_{(\emptyset)} = 0$ .

to it and after only a small amount of training applied it successfully to a number of problems. Thus it seems that this algorithm together with its counterpart, the supermesh analysis (for nullor circuits), has reached a state of maturity, that makes it perfectly suitable for presentation as "universal tools" in any course on circuit theory.

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#### NOTE ADDED TO THE ELECTRONIC VERSION

In this electronic document, some small typographical errors of the printed version were corrected. The figures, though still drawn by hand, now are from the original coloured drawings.

Furthermore, for the convenience of the reader the abstract has been rewritten, and keywords, ACM and MSC classifications, and a short CV according to IEEE standards have been added. One URL has been added to the bibliography.  
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